ABSTRACT

An integrated circuit device package with a first part (101) having a cavity (104) to mount the chip (105), further I/O terminals (102) on the top surface and terminals (103) on the bottom surface. The chip has contact pads (107a and 107b). The second part (110) of the package has bottom surface terminals (111) aligned with the chip contact pads, and bottom terminals (112) aligned with the terminals (102) of the first package part. The connections are provided by stud bumps between the chip contact pads and terminals (111), and by reflow material between terminals (102) and (112). The connector lines (109a and 109b) in the second package part (110) comprise signal/power and ground layers. The layers are spaced by insulation between 10 and 50 μm thick, and the connector lines have a width less than three times the insulator thickness.